L Number	Hits	Search Text	DB	Time stamp
1	5	(("4,954,951") or ("5,083,265") or ("5,459,846") or ("5,841,947") or ("6,071,317")).PN.	USPAT; US-PGPUB	2003/10/19 20:03

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Computing at Cambridge

... of course) which accepted **machine code** programs in ... the first thoughts I can recall
about **Artificial Intelligence**. ... subsequently be able to **generate** good English ...
www.rbjones.com/rbjpub/rbjcv/rjiab/rjiab004.htm - 7k - Cached - Similar pages

[PDF]A06507 THE UNIVERSITY OF BIRMINGHAM Degree of B.Sc. with Honours ...

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... **Artificial Intelligence** and Computer Science ... are held in memory, and consider this
expression: x + (y + (z + 42)) (a) **Generate** stack **machine code** for the ...
www.cs.bham.ac.uk/~hxt/teaching/compilers2004/ 2002-compiler-exam.pdf - Similar pages

User-Modelling in **Artificial Intelligence** and Human-Computer ...

... program was less efficient than **machine code** and required ... for the human user to **generate**
a program ... Research in **artificial intelligence** has been primarily based ...
www.io.com/~jwtlai/usermodel.html - 29k - Cached - Similar pages

Natural Language Processing

... We have the ability to **generate** sentences that are ... Research in AI (**Artificial Intelligence**) has been ... English (etc) <--- **machine code**; sign language <---> voice; ...
infocom.cqu.edu.au/Staff/Owen_Van-Itallie/Research/ Artificial_Intelligence/Talking_to_Computers/ - 47k - Cached - Similar pages

Automatic Derivation of Code Generators from Machine Descriptions

... 25 REISER, J., ET AL. SAIL Stanford **Artificial Intelligence** Lab. Memo. ... 33 Wmcox, TR Generating **machine code** for high-level programming languages. ...
portal.acm.org/ citation.cfm?id=357097&jmp=abstract&dl=GUIDE&dl=ACM&CFID=11111111&CFTO... - Similar pages

Evolution of Complexity

... present our experiments in utilizing evolution to **generate** complexity in ... the dawn of the era of true **artificial intelligence**. ... Tierran genomes are **machine code**. ...
www.isd.atr.co.jp/~ray/pubs/atrjournal/ - 14k - Cached - Similar pages

Why Poplog Pop-11 was never implemented in C

... compiler which has to **generate machine code** for the ... However, instead of generating **machine code** directly from ... Science Volume 5: **Artificial Intelligence**, eds D ...
www.poplog.org/talk/comp.lang.pop/1993/msg00164.html - 12k - Cached - Similar pages

Evolutionary and Adaptive Systems (EASy) at Sussex

... I argue that the use of **Artificial Intelligence** techniques such ... The **machine code** evolution system is found to ... be the starting point to **generate** cell boundaries ...
www.cogs.susx.ac.uk/easy/Publications/ MScTheses1999.html - 25k - Cached - Similar pages

Dept. of AI:
... **generate** efficient code that compares to unverified compilers. ... ie the correct transformation of the compiling specification to **machine code** of the compiler ...
www.informatik.uni-ulm.de/ki/verifix.html - 21k - Cached - Similar pages

Courses - Undergraduate - CS - Programs - Baskin School of ...
... Students **generate machine code** runnable on a real machine. Prerequisite(s): course 104A. D. Long, W. Mackey. 105. ... 140. **Artificial Intelligence**. ...
www.cse.ucsc.edu/programs/cs/ undergraduate/courses.html - 43k - Oct 18, 2003 - Cached - Similar pages

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Linux AI & Alife HOWTO: Programming languages

... used extensively for, if not specifically made for, **artificial intelligence** programming. ... C
can then compiled with a normal C compiler to **generate machine code**. ...
new.linuxnow.com/docs/content/AI-Alife-HOWTO-html/ AI-Alife-HOWTO-7.html - 22k - Cached - Similar pages

[PDF]Artificial Intelligence and Robotics SIG Official Journal October ...

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... in computer science at the MIT **Artificial Intelligence** Laboratory where ... diagrams are
used to automatically **generate** code ... the Lisp Code to **machine code** to drive ...
www.airobotics.org/archive/newsletter1.pdf - Similar pages

Kurzweil Technologies, Inc.: Publications

... rules (the "genetic code") to **generate** subsequent generations ... Specifically, in **artificial**
intelligence, the rapid growth in ... that produces a **machine code** from a ...
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Generations of Programming Languages

... Assembly or **machine code** could not run on different ... used in the field of **artificial intelligence**, fuzzy logic ... to use product that can **generate** new applications ...
www-dse.doc.ic.ac.uk/~nd/surprise_96/ journal/vol2/mjbn/article2.html - 11k - Cached - Similar pages

Digital Burgess - Program

... consists of bits of **machine code** that act as ... Larry Yaeger approaches **artificial intelligence** the same way ... and since intelligent systems **generate** such complexity ...
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Artificial Intelligence Artificial Intelligenc...

... views of Noam Chomsky, to the study of **Artificial Intelligence**. ... that can be used to **generate** all the ... be converted to a universal human '**machine code**.'" From a ...
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Artificial Intelligence

... views of Noam Chomsky, to the study of **Artificial Intelligence**. ... that can be used to **generate** all the ... be converted to a universal human '**machine code**.' From a ...
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... How Can **Artificial Intelligence** Help Us? ... This means that the **machine code** can be mutated(by flipping ... **Generate** database-driven Web applications in ASP, PHP, JSP ...
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... Design Handbook: Optimizations & **Machine Code** Generation By ... Clauses (Lecture Notes in **Artificial Intelligence**) By: Matthew ... Can **generate** C code or Java bytecode. ...
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What .NET and Visual Studio are All About

... **Artificial Intelligence** Center. ... that under .NET, the .EXE files don't contain Pentium **machine code**! ... They **generate** rather large .EXE files which call lower-level ...
www.ai.uga.edu/mc/DotNet/ - 15k - Cached - Similar pages

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Package: lang/lisp/impl/clicc/

CMU **Artificial Intelligence** Repository Home INFO Search FAQs ... library in order to **generate**
executables. ... translation of abstract **machine code** to corresponding C ...
www.cs.cmu.edu/afs/cs/project/ai-repository/ ai/lang/lisp/impl/clicc/0.html - 4k - Oct 18, 2003 - Cached - Similar pages

Generating Decision Trees for Decoding Binaries

... a tool can use to **generate** a decoder. ... The New Jersey **Machine-Code** Toolkit, Reference
Manual, 1996. ... J. Russell , Peter Norvig, **Artificial intelligence**: a modern ...
portal.acm.org/
citation.cfm?id=384213&jmp=references&dl=portal&dl=ACM&CFID=11111111&C...
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dependency ...
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Supporting dynamic languages on the Java virtual machine

Olin Shivers MIT **Artificial Intelligence** Laboratory April 25, 1996 ... the macro-expanders to **generate** safe uses ... source and processor-specific **machine code** do not ...
www.ai.mit.edu/~shivers/javaScheme.html - 24k - Cached - Similar pages

Nat'l Academies Press, Roles of Industry and the University in ...

... are needed for the generation of **machine code** because of ... of the field known as **artificial intelligence** (AI). ... scenes how to understand and **generate** speech or ...
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... **Artificial intelligence**. ... **Generate** intermediate text. ... find patterns in intermediate text, match with templates, produce corresponding **machine code**. ...
www.cse.scu.edu/~rdaniels/html/courses/ Coen171/Preliminaries.ppt - Similar pages

New Scientist | AI and A-Life | A life in silicon

... computer programmer from the **Artificial Intelligence** Laboratory at ... tiny, self-replicating **machine code** programs, which ... and the ones that **generate** error messages ...
www.newscientist.com/hottopics/ai/lifeinsilicon.jsp - 29k - Oct 18, 2003 - Cached - Similar pages

§8 The Research of **Artificial Intelligence** Model and Brain ...

... 4. The model can **generate** a new machine ... For various **artificial intelligence** models and neuron models, from the ... have three periods: the **machine code** period, the ...

www.holotopology.org/thepage/pageb8.htm - 35k - Cached - Similar pages

AAEZ Robot Project

... Nets and Description Matching; **Generate** and test ... for the CS547 Graduate level **Artificial Intelligence** course taken ... Stack **machine code** tends to be smaller than a ...
www.wiu.edu/users/muaa/proj/robot.htm - 15k - Cached - Similar pages

1 Introduction to **Artificial Intelligence**

... a machine understand and **generate** human language ... as they pertain to **Artificial Intelligence** operate at a ... the most thorough understanding of arcane **machine code**. ...
www.compapp.dcu.ie/~tonyv/Textbook/history.html - 101k - Cached - Similar pages

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Books

... increases are demonstrated by directly evolving **machine code**, and implementation ... defined
functions, evolving logic programs that **generate** recursive structures ...
www.geneticprogramming.com/GPpages/books.html - 32k - Cached - Similar pages

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... Code generation. **Generate machine code**. Lexical analysis. Keywords. ... Digital rights
management. Access to information (Digital Divide). **Artificial intelligence**.
www.cs.princeton.edu/courses/archive/spr02/cs111/Lectures/Lecture13ProgrammingII.ppt - Similar pages

[PDF]Robotics and **Artificial Intelligence** by Dr Clarence Tan School of ...

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... compiled on microcomputers into the **machine code** for the ... **Artificial intelligence** algorithms
in pattern recognition and image ... an assembly robot to **generate** a 4 ...
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Module and Programme Catalogue

... the concepts of compilation and **machine code**. ... string manipulation commands to **generate** inquiries in ... the possibility of **Artificial Intelligence** and Artificial ...
www.leeds.ac.uk/students/ugmodules/acom1910.htm - 13k - Oct 18, 2003 - Cached - Similar pages

[PDF]Principles of Programming Languages Project manager's dilemma ...

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... n Business (Cobol) n "**artificial intelligence**" (Lisp, Scheme ... code Optimizer
Code generator **Machine code** Source program ... n They need not **generate** code but ...
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... structure and command set as **machine code** but they ... and the report to **generate** then turned ... emphasis on human-computer interaction and **artificial intelligence**. ...
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[DOC]Mohammad Al Hasan

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... It can compile a C-- code to **generate** MIPS **machine code**. ... Communication, Compiler Design, Computer Graphics, **Artificial Intelligence**, Computer Architecture ...
www-users.cs.umn.edu/~mhasan/new2.doc - Similar pages

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... theory we use to **generate** the research ... as well as the **machine code** became available

to ... experienced programmer at MIT's **Artificial Intelligence** Laboratory, were ...
sspaeth.org/tmp/freenet4.9.ps - Similar pages

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... called a compiler) converts the high level code to **machine code**. ... Scheme: good for **artificial intelligence**. ... Dev C++ will automatically **generate** most of the code. ...
www.sfusd.k12.ca.us/schwww/sch697/ depts/math/simon/c2.ppt - Similar pages

Tutorials

... or efficient on-the-fly translation to **machine-code** for execution ... Ada 95 front end ("AdaMagic"(tm)) to directly **generate** J-code ... **Artificial Intelligence** with Ada. ...
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... is added to the new **database** one by one ... called TrapDis- patcher into this low-memory
exception vector. ... the dispatch number following the TRAP **op- code**, and uses ...
examples.oreilly.com/palmpilot2/Palm_OS_Emulator_Win/ Docs/12rollin.pdf - Similar pages

Exception Handling and Computer Security
... an error such as an illegal **op-code**, it calls ... processor and that region belongs to the **database**. ... unique longword location in the **exception vector** table located ...
wheelie.tees.ac.uk/users/a.clements/ Excepts/Excepts.htm - 92k - Cached - Similar pages

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1 Motorola 68040 microprocessor simulation for the Sun Workstation
Trey Grubbs, Bill Herring, Richard Tan, Susan Mengel
April 1994 Proceedings of the 1994 ACM symposium on Applied computing
Full text available: pdf(769.14 KB) Additional Information: full citation, references, index terms

Keywords: computer aided instruction, microprocessr simulators

2 A 16-bit microprocessor with multi-register bank architecture
Hideo Maejima, Hiroyuki Kida, Tan Watanabe, Shiro Baba, Keiichi Kurakazu
November 1999 Proceedings of 1986 fall joint computer conference on Fall joint cc
Full text available: pdf(500.78 KB) Additional Information: full citation, references, index tern

3 Just what is an op-code?: or a universal computer design
James Brakefield
June 1982 ACM SIGARCH Computer Architecture News, Volume 10 Issue 4
Full text available: pdf(276.18 KB) Additional Information: full citation, abstra

The following computer architecture offers extensible machine language. Tha does this by using the same format for both op-codes and subroutine calls. Tl programmer can chose an instruction set for the application at hand. Ie., the program can correspond to a high level textual representation or a program.T this architecture is essentially a w ...

4 The internal machine
Andrew M. Welin
November 1973 Proceedings of the ACM-IEEE symposium on High-level-languag
Full text available: pdf(740.42 KB) Additional Information: full citation, abstract, referer

Two results are presented in this paper: an enlargement of the concept of ma computers based on an inner machine oriented toward interpretation of mach discuss attributes of “directly interpretable languages” and proc interpretation. “Sequential extraction” allows an instruction to l decoding” allows us to organize t ...

5 Affix grammar driven code generation
Mahadevan Ganapathi, Charles N. Fischer
October 1985 ACM Transactions on Programming Languages and Systems (TOP
Full text available: pdf(3.19 MB) Additional Information: full citation, abstract, references, citi

Affix grammars are used to describe the instruction set of a target architectu A code generator is obtained automatically for a compiler using attributed pa model can automatically perform most popular machine-dependent optimizat Code generators based on this model demonstrate retargetability for the VAX

6 A novel approach to character interfaces
Robert Cousins
March 1990 ACM SIGARCH Computer Architecture News, Volume 18 Issue 1
Full text available: pdf(541.04 KB) Additional Information: full citation, index terms

7 Verification of microprogrammed computer architectures in the S*-system:
W. Damm, G. Dohmen
December 1985 ACM SIGMICRO Newsletter , Proceedings of the 18th annual work:
Issue 4
Full text available: pdf(1.43 MB) Additional Information: full citation, abstract, referen

We apply the verification methodology underlying the S*-System[12], [13] t structured design [16] of an emulation of the instruction-set of a commercial available micro-architecture. Based on this case-study, we discuss some aspe generation of microcode.

8 Computer-assisted instruction: Specification of attributes for CAI programs
Gloria M. Silvern, Leonard C. Silvern
January 1966 Proceedings of the 1966 21st national conference
Full text available: pdf(1.15 MB) Additional Information: full citation, abstract, references,

Man's search for knowledge began in antiquity and led ultimately to the inve book of 72 pages, was published in 15961. It contained spelling lessons and short catechism. The first American textbook was published in 1641. This is r press in the colonies, assembled only a few years before, in 1639. Nearly 20(

9 Coding isomorphisms
William C. Lynch
February 1960 Communications of the ACM, Volume 3 Issue 2
Full text available: pdf(263.22 KB) Additional Information: full citation, abstr

The coding of external symbols into symbols internal to a computer can some relevant informational properties are preserved, but in a form much more eas

10 Introducing computer concepts by simulating a simple computer
Robert A. Campbell
September 1996 ACM SIGCSE Bulletin, Volume 28 Issue 3
Full text available: pdf(217.65 KB) Additional Information: full citation, abstract, cit

The simulated computer consists of (1) main memory, (2) a register known a unit (CPU), and (4) an instruction counter. This computer recognizes 8 op coc Write, and Branch On Zero). The computer is simulated by creating a prograr the execution of programs written by students, such as adding two numbers are written in machine langua ...

11 BASICI—a simple computer to introduce computer organization and
Donald S. Miller, Bruce R. Millard
February 1982 Proceedings of the thirteenth SIGCSE technical symposium on Co
Full text available: pdf(791.01 KB) Additional Information: full citation, abstract,

BASICI is a simple interactive assembler-loader/interpreter which has been u: introductory course in computer organization and assembler language progra Department at Washington State University. Both “hardware” a emphasize basic concepts and to eliminate the confusion which occurs when surrounded by the myriad of machine and assembler lan ...

12 An analysis of 8086 instruction set usage in MS DOS programs
T. L. Adams, R. E. Zimmerman
April 1989 ACM SIGARCH Computer Architecture News , Proceedings of the third i support for programming languages and operating systems, Volume 1
Full text available: pdf(943.30 KB) Additional Information: full citation, references, c

13 The Cornell program synthesizer: a syntax-directed programming environm
Tim Teitelbaum, Thomas Reps
September 1981 Communications of the ACM, Volume 24 Issue 9
Full text available: pdf(1.12 MB) Additional Information: full citation, abstract, references,

Programs are not text; they are hierarchical compositions of computational st and debugged in an environment that consistently acknowledges and reinforc Synthesizer demands a structural perspective at all stages of program develo a common foundation: a grammar for the programming language. Its full-scr syntax-directed diagnostic interpreter c ...

Keywords: diagnostic interpreter, program development system, programmin syntax-directed editor, template

14 MICROSIM: A microinstruction simulator for teaching microprogramming a
Francis P. Mathur
October 1977 Proceedings of the 10th annual workshop on Microprogramm
Full text available: pdf(753.43 KB) Additional Information: full citation, abstract, refer

This paper describes in the format of a user's manual, along with an example and emulation. This program simulates at the microinstruction set level the a microprogram-controlled minicomputer. This simulator, as an instructional ve software engineering laboratory adjunct to a regular course in microprogramr

15 ABLE: A LISP-based layout modeling language with user-definable proced design
Gary B. Goates, Suhas S. Patil
June 1981 Proceedings of the eighteenth design automation conference on De
Full text available: pdf(692.32 KB) Additional Information: full citation, abstract, refere

ABLE, an array-based linguistic editor, is a layout modeling language for stor the LISP programming language. This paper describes ABLE's design, present ABLE's usefulness in SLA-based circuit design. ABLE embodies a linguistic ap very large scale integrated (VLSI) circuits; digital system designers can repre relatively abstract and hi ...

16 Modeling and control of robotic mine haulage system
Ernest G. Holzmann, Kenneth B. Haefner
March 1982 Proceedings of the fifteenth annual simulation symposium
Full text available: pdf(1.03 MB) Additional Information: full citation, abstract,

Concepts borrowed from discrete and hybrid system simulation have been su complex, distributed computer control system. The example presented is a ra mine. The system controls all train movements and haulage operations into a embedded in the system software, distributed over three levels: 1. Central cc Wayside co ...

17 Address size independence in a 16-bit minicomputer
Philip E. Stanley
April 1978 Proceedings of the 5th annual symposium on Computer architect
Full text available: pdf(648.93 KB) Additional Information: full citation, abstract, refer

Most minicomputers do not distinguish in their architecture between addresse operand size becomes a de facto limit on address size (and thus memory size many architectures when attempting to build systems with large address spa size “invisible” to the programmer and independent of operand,

18 Retargetable Compiler Code Generation
Mahadevan Ganapathi, Charles N. Fischer, John L. Hennessy
December 1982 ACM Computing Surveys (CSUR), Volume 14 Issue 4
Full text available: pdf(1.93 MB) Additional Information: full citation, references, citings, index terms

19 The contribution to performance of instruction set usage in System/370
O. R. LaMaire, W. W. White
November 1999 Proceedings of 1986 fall joint computer conference on Fall joint cc
Full text available: pdf(1.18 MB) Additional Information: full citation, references, citings, index te

20 A verification technique for gated clock

Masamichi Kawarabayashi, Narendra Shenoy, Alberto Sangiovanni-Vincentelli

July 1993 Proceedings of the 30th international on Design automation conference

Full text available: pdf(577.49 KB) Additional Information: full citation, references, citings, index terms

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21 The George Washington University Core System implementation
James D. Foley, Patricia A. Wenner
August 1981 Proceedings of the 8th annual conference on Computer graphics a
Full text available: pdf(728.20 KB) Additional Information: full citation, abstract, referenc

A full implementation of the proposed standard Core System graphics subrou described. Emphasis is placed on the internal structure of the implementatior features of the implementation include separate 2D and 3D viewing pipelines flow of information between various parts of the Core, a strong separation be device-dependent parts of t ...

22 Storage concepts in a software-reliability-directed computer architecture
Glenford J. Myers
April 1978 Proceedings of the 5th annual symposium on Computer architecti
Full text available: pdf(513.49 KB) Additional Information: full citation, abstract, referenc

Because of the tremendous difficulty of producing reliable software (applicati consequences of software errors, a new solution is being explored: the devel will substantially enhance the reliability of the programs executing above it. concepts (e.g., data representations and addressing) in the architecture.

23 Graphics language / one - IBM Corporate-Wide physical design data forma
David R. Lambert
June 1981 Proceedings of the eighteenth design automation conference on De
Full text available: pdf(392.15 KB) Additional Information: full citation, abstract, reference

The evolution and structure of the IBM Corporate-Wide physical design data l is discussed. The need for a common graphics interface for communication ar is demonstrated. At IBM, the same format is used from physical layout to ma printed circuit board designs.

24 Packed scatter tables
Gordon Lyon
October 1978 Communications of the ACM, Volume 21 Issue 10
Full text available: pdf(834.68 KB) Additional Information: full citation, abstract, reference

Scatter tables for open addressing benefit from recursive entry displacements auxiliary cost functions. Compared with conventional methods, the new techr that resemble exact-solution optimal packings. The displacements are depth- (exhaustive) optimization, although packing costs remain linear—O(n) Keywords: assignment problem, backtrack programming, hashing, open addr rearrangements

25 The basic side of tape labeling
William A. Logan
February 1960 Communications of the ACM, Volume 3 Issue 2
Full text available: pdf(214.14 KB) Additional Information: full citation, ab

Once an installation has determined that it would be advantageous to be able reel of tape on hand and to be able to check those identifications by program Labeling Routine. The parameters of such a routine are limited only by the in installation as they request (and frequently demand) that the label on the tap tallies, messages, rem ...

26 Optimizing direct threaded code by selective inlining
Ian Piumarta, Fabio Riccardi
May 1998 ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 1998 confere implementation, Volume 33 Issue 5
Full text available: pdf(1.28 MB) Additional Information: full citation, abstract,

Achieving good performance in bytecoded language interpreters is difficult wi portability. This is due to the complexity of dynamic translation ("just-in-time code, which is the mechanism employed universally by high-performance int techniques make it possible to create highly-portable dynamic translators tha performance of optimized C for certain n ...

Keywords: bytecode interpretation, dynamic translation, inlining, just-in-time

27 Simulation structure for the development of Texas Instruments' Advanced S
Sidney D. Nolte, Marvin T. Talbott
June 1973 Proceedings of the 1973 symposium on Simulation of computer sy
Full text available: pdf(1.10 MB) Additional Information: full citation, abstract, referenc

During development of a large-scale computer system, design decisions must experience. As development continues past the design phase, it is necessary subsystem is doing what it was designed to do from both functional and perfc necessary to have some means of evaluating the effects of proposed changes tool in satisfying ...

28 The implementation of a user-extensible system on a dynamically microprc
Fergus K. Fung, Willis K. King
October 1977 Proceedings of the 10th annual workshop on Microprogramm
Full text available: pdf(308.59 KB) Additional Information: full citation, abstract, refere

On a dynamically user-microprogrammable computer the user can tailor the i microprogrammed routines and adding them to the system. If these routines using them is no different from using any other basic machine instruction of t extended. The design and implementation of such a user-extensible system i: pager which manages a virtual memory fo ...

29 Contemporary Concepts of Microprogramming and Emulation
Robert F. Rosin
December 1969 ACM Computing Surveys (CSUR), Volume 1 Issue 4
Full text available: pdf(1.40 MB) Additional Information: full citation, references, citings, index terms

30 Hardware and software support for efficient exception handling
Chandramohan A. Thekkath, Henry M. Levy
November 1994 Proceedings of the sixth international conference on Architectural operating systems, Volume 29 , 28 Issue 11 , 5
Full text available: pdf(1.44 MB) Additional Information: full citation, abstract, references

Program-synchronous exceptions, for example, breakpoints, watchpoints, illeg provide information about exceptional conditions, interrupting the program a handler. Over the last decade, however, programs and run-time systems hav as a performance optimization to detect normal and expected conditions. Unf

31 An architectural framework for migration from CISC to higher performance
Gabriel M. Silberman, Kemal Ebcio?lu
August 1992 Proceedings of the 6th international conference on Supercomp
Full text available: pdf(2.04 MB) Additional Information: full citation, abstract, references,

We describe a novel architectural framework that allows software applications Set Computer (CISC) to migrate to a different, higher performance architectu part of the application user or developer. The framework provides a hardware between two instruction sets, resulting in a machine that enhances applicatio program behavior (from a user per ...

32 Hardware combining and scalability
Susan R. Dickey, Richard Kenner
June 1992 Proceedings of the fourth annual ACM symposium on Parallel algorithn
Full text available: pdf(967.92 KB) Additional Information: full citation, references, citings, index

33 META II a syntax-oriented compiler writing language
D. V. Schorre
January 1964 Proceedings of the 1964 19th ACM national conference
Full text available: pdf(782.31 KB) Additional Information: full citation, abstract, reference

META II is a compiler writing language which consists of syntax equations res which instructions to output assembly language commands are inserted. Com for VALGOL I and VALGOL II. The former is a simple algebraic language desig The latter contains a fairly large subset of ALGOL 60. The method of writing c paper may be expl ...

34 A MULTILINGUAL INTERPRETER for interactive computing in an academ
Larry Kheriaty
August 1973 Proceedings of the annual conference
Full text available: pdf(381.53 KB) Additional Information: full citation, abstra

In order to satisfy three types of terminal users, student programmers, produ Washington State College has developed a MULTILINGUAL INTERPRETER. The BASIC and COURSEWRITER III to be run on a single terminal system. The co such that programs can be prepared in more than one source language. The r provide advanced programming features not only ...

35 A microcoded real-time executive for numeric support nodes distributed wi
J. O. Bondi
January 1988 Proceedings of the 21st annual workshop on Microprogramming a
Full text available: pdf(305.46 KB) Additional Information: full citation, abstract, reference

The mix of nodes within heterogeneous embedded networks typically include oriented nodes particularly adept at efficient manipulation of regularly structu “Array Processing” (AP) nodes usually serve other more genera control of each AP is maintained by a microcoded AP-resident executive progr and tuned to minimize ...

36 Enabling trusted software integrity
Darko Kirovski, Milenko Drini?, Miodrag Potkonjak
October 2002 Tenth international conference on architectural support for program Proceedings of the 10th international conference on architectural su operating systems (ASPLOS-X), Volume 37 , 30 , 36 Issue 10 , 5 ,
Full text available: pdf(1.39 MB) Additional Information: full citation, abstract

Preventing execution of unauthorized software on a given computer plays a p problem is that although a program at the beginning of its execution can be v execution flow can be redirected to externally injected malicious code using, Existing techniques address this problem by trying to detect the intrusion at r software is not prone to a p ...

37 Description-driven code generation using attribute grammars
Mahadevan Ganapathi, Charles N. Fischer
January 1982 Proceedings of the 9th ACM SIGPLAN-SIGACT symposium on Princ
Full text available: pdf(988.59 KB) Additional Information: full citation, abstra

The instruction-set of a target architecture is represented as a set of attribute obtained automatically for any compiler using attributed parsing techniques. automatically perform most popular machine-dependent optimizations, incluc generator is also easily retargetable to different machine architectures.

38 High-level power estimation (invited talks): A multi-level strategy for softwa
C. Brandolese, W. Fornaciari, L. Pomante, F. Salice, D. Sciuto
September 2000 Proceedings of the 13th international symposium on Syster
Full text available: pdf(117.56 KB) Additional Information: full citati

In this paper a comprehensive methodology for software power estimation is by rigorous mathematical models of power consumption at three different lev been validated in a complete framework developed within the TOSCA co-desi

39 An example RISC vector machine architecture
Martin Dowd
September 1987 ACM SIGARCH Computer Architecture News, Volume 15 Issue 4
Full text available: pdf(484.57 KB) Additional Information: full citation, index terms

40 Interleaving: a multithreading technique targeting multiprocessors and worl
James Laudon, Anoop Gupta, Mark Horowitz
November 1994 Proceedings of the sixth international conference on Architectural operating systems, Volume 29 , 28 Issue 11 , 5
Full text available: pdf(1.35 MB) Additional Information: full citation, abstract, references

There is an increasing trend to use commodity microprocessors as the compu However, given that the majority of the microprocessors are sold in the work market, it is only natural that architectural features that benefit only multipr commodity microprocessors. In this paper, we explore multiple-context proce to hide the large me ...

Results 41 - 60 of 151 Result page: previous 1 2 **3** 4 5 6

41 Design tradeoffs for software-managed TLBs

Richard Uhlig, David Nagle, Tim Stanley, Trevor Mudge, Stuart Sechrest, Richar
August 1994 ACM Transactions on Computer Systems (TOCS), Volume 12 I

Full text available: pdf(1.85 MB) Additional Information: full citation, abstract, references, citi

An increasing number of architectures provide virtual memory support throug software management can impose considerable penalties that are highly dep and its use of virtual memory. This work explores software-managed TLB des range of monolithic and microkernel operating systems. Through hardware m performance for benchmarks running on a ...

Keywords: hardware monitoring, translation lookaside buffer (TLB), trap-driv

42 Delta storage for arbitrary non-text files

Christoph Reichenberger
May 1991 Proceedings of the 3rd international workshop on Software configuratic

Full text available: pdf(634.58 KB) Additional Information: full citation, references, citings, index te

43 An Efficient Compiler Technique for Code Size Reduction Using Reduced I
A. Halambi, A. Shrivastava, P. Biswas, N. Dutt, A. Nicolau
March 2002 Proceedings of the conference on Design, automation and test ir
Full text available: pdf(289.61 KB) Publisher Site Additional Infor

For many embedded applications, program code sizeis a critical design factor. size is to employ a "dual instruction set",where processor architectures suppo and a narrow, space-efficient(usually 16 bit) Instruction Set with a limited se registers. This feature, however, requires compilers that can reduce codesize Existingcompiler ...

44 An advanced tactical computer concept
Kenneth J. Thurber, Peter C. Patton, Robert C. Deward, Jon C. Strauss, Thomas
March 1977 ACM SIGARCH Computer Architecture News , Proceedings of the 4th a architecture, Volume 5 Issue 7
Full text available: pdf(432.42 KB) Additional Information: full citation, abstract, refer

This paper discusses the design of a real-time computer. The computer's desi architecture are summarized. The paper discusses how the design requireme The system's three upward compatible addressing options (real, base, virtual

45 Micro emulation: When to do it and when not to do it
Lee Hoevel
September 1973 Conference record of the 6th annual workshop on Micropro
Full text available: pdf(723.79 KB) Additional Information: full citation, abstract, refer

In this paper, we will attempt to analyze those conditions under which the us the performance of a two-phase processing system. This analysis is couched “ideal” DEL, given a particular source language SL and base ma would minimize the overall space and time needed to evaluate a typical SL p

46 Teaching basic computer organization through “microprogramming&
Miriam R. Tausner
September 1973 Conference record of the 6th annual workshop on Micropro
Full text available: pdf(170.19 KB) Additional Information: full citation, abstract, cit

To reinforce concepts of CPU organization students are asked to write a &ldqu be run on a theoretical microprogrammable computer which is simulated usir

47 Direct microprogrammed execution of the intermediate text from a high-lev
Francois Robert Broca, Richard E. Merwin
May 1973 Proceedings of the meeting on SIGPLAN/SIGMICRO interface
Full text available: pdf(654.98 KB) Additional Information: full citation, abstract, references

Microprogramming commonly executed operations can improve the computat This paper describes how microprogramming may be used to execute directly high-level language compiler after syntactic and semantic analysis of the inpı microprogrammed execution of common forms of intermediate text - i.e.: qu simulated. A comparison is made, in terms of sto ...

48 Representation: Out-of-core encoding of large tetrahedral meshes
Shyh-Kuang Ueng
July 2003 Proceedings of the 2003 Eurographics/IEEE TVCG Workshop on Volu
Full text available: pdf(210.67 KB) Additional Information: full citation, abstract, refer

In this paper, an out-of-core data compression method is presented to encod meshes. The method is comprised with two stages. At the first stage, the inpı octants, based on an octree structure. Each octant must contain less FEA cell into the main memory. Octants produced in the data division are stored in di traversed to enumerate ...

49 Direct microprogrammed execution of the intermediate text from a high-lev
Francois Robert Broca, Richard E. Merwin
August 1973 Proceedings of the annual conference
Full text available: pdf(521.76 KB) Additional Information: full citation, abstract, references

Microprogramming commonly executed operations can improve the computat This paper describes how microprogramming may be used to execute directly high-level language compiler after syntactic and semantic analysis of the inpı microprogrammed execution of common forms of intermediate text - i.e.: qu simulated. A comparison is made, in terms of sto ...

50 Languages for direct execution
Lee W. Hoevel
September 1974 Conference record of the 7th annual workshop on Micropro
Full text available: pdf(775.94 KB) Additional Information: full citation, abstract, refer

The utility of a modern computing system lies in its capacity to perform a var user control. In the earliest systems users exerted direct, low-level control, ir applied to a data item manually at the time it was to be performed—ir controls a small electronic calculator. With the passage of time, this user con sophisticated, culminating in th ...

51 Micro control hardware and high level languages interpretor: An attempt of
J. Demarteau
September 1974 Conference record of the 7th annual workshop on Micropro
Full text available: pdf(512.38 KB) Additional Information: full citation, abstract, refer

The aim of this paper is to try and describe a new technique for implementin interpretor of macro-languages. It demonstrates the connexion between the micro-instruction and the structure of a dynamic interpretor. The proposed m fetch/generator instruction (1), is founded on a microprocedure call generato of the CPU are split into two specific levels : t ...

Keywords: Address control, Architecture, Instruction-generator, Macro-genera

52 A logical approach to teach digital computer design at logic and systems le
Sarma R. Vishnubhotla
February 1977 Proceedings of the seventh SIGCSE technical symposium on Con
Full text available: pdf(473.90 KB) Additional Information: full citation, abstra

Design courses in Computer Systems Design are being taught in many under Science and Electrical Engineering students. A design project is explained in students regarding the important concepts in both logic and systems level. TI memory and a single index register. This project can also be enlarged by intr

53 MBALM/1700: A microprogrammed LISP machine for the Burroughs B172
M. L. Griss, M. R. Swanson
October 1977 Proceedings of the 10th annual workshop on Microprogramm
Full text available: pdf(1.02 MB) Additional Information: full citation, abstract, references,

This paper describes the implementation of BALM and LISP processors for the processors consist of an interpreter of MBALM pseudo-code (written in MIL), code (written in BALM or LISP). Of particular interest is the modular design o to evaluate and improve the size and speed of the machine. The current syst compilation, compacting garbag ...

54 Evolution in the design of abstract machines for software portability
Daniel Thalmann
May 1978 Proceedings of the 3rd international conference on Software engin
Full text available: pdf(535.40 KB) Additional Information: full citation, abstract, referenc

The abstract machine model is the best one for solving the difficult problem the design of these machines is necessary. After a brief survey of the well-kn the design of a more general one to implement portable operating systems. T abstract machine to existing computers is discussed and the paper explains h inestimable means to reduce the ...

55 Design of a Lisp machine - FLATS

E. Goto, T. Soma, N. Inada, T. Ida, M. Idesawa, K. Hiraki, M. Suzuki, K. Shimizu

August 1982 Proceedings of the 1982 ACM symposium on LISP and functional

Full text available: pdf(501.49 KB) Additional Information: full citation, abstract, reference

Design of a 10 MIPS Lisp machine used for symbolic algebra is presented. Be mechanisms which greatly speed up primitive Lisp operations, the machine is for content addressed associative tabulation and a very fast multiplier for spe fast hash address generation.

56 Compiler chip: A hardware implementation of compiler

Akira Fusaoka, Masaharu Hirayama

March 1982 Proceedings of the first international symposium on Architectural sup operating systems

Full text available: pdf(301.61 KB) Additional Information: full citation, abstract, refer

In this paper we discuss about another approch: Compiler Chip, which is a VL Constructing a compiler by a few VLSI chip, the computer manufacturer can c these chips are installed in a intelligent terminal in order to remove the comp in the mainframe.

57 An experiment to improve operand addressing

Robert P. Cook, Nitin Donde

March 1982 Proceedings of the first international symposium on Architectural sup operating systems

Full text available: pdf(398.18 KB) Additional Information: full citation, abstract, refer

MCODE is a high-level language, stack machine designed to support strongly variety of data types in a modular programming environment. The instructior extensibility, is based on an analysis of 120,000 lines of Pascal programs. Th the instruction sets of the Digital Equipment PDP-11 and VAX by examining t for all three machines. In addition ...

Keywords: Addressing modes, Computer architecture, Stack machine

58 A Metafile for efficient sequential and random display of graphics
Theodore N. Reed
July 1982 Proceedings of the 9th annual conference on Computer graphics and
Full text available: pdf(386.23 KB) Additional Information: full citation, abstract, refer

Graphics metafiles have been in use at the Los Alamos National Laboratory si was defined in 1976 and has been updated several times to allow efficient gr environment. History and current applications of the Common Graphics Syste objectives, details of the format, and random access extensions incorporated

Keywords: Device-independent, Metafile, Random access

59 Computer-1—a modern simple computer to introduce computer org programming
Donald S. Miller
February 1983 Proceedings of the fourteenth SIGCSE technical symposium on C
Full text available: pdf(537.52 KB) Additional Information: full citation, abstract

COMPUTER-1 is an interactive editor/assembler simulator-debugger and prog instructional tool for an introductory course in computer organization and ass COMPUTER-1's organization, assembler language and interactive facilities are computer architecture and assembly language programming while minimizing dependent details present during this learning period. COMPUTER- ...

60 Structured design verification: Function and timing
C. J. Rimkus, M. R. Wayne, D. D. Cheng, F. J. Magistro
June 1983 Proceedings of the twentieth design automation conference on Des
Full text available: pdf(569.17 KB) Additional Information: full citation, abstract, reference

Changes in the design verification environment brought about by VLSI desigr modelling support is now required of efficient, interactive verification tools. T environment is analyzed, especially in early error removal during the design been implemented as part of the IBM Design and Verification system, is desc the key areas of hie ...

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1 **Machine code generating to speed-up the circuit simulation**
Chitcharus, N.; Leelarasmee, E.;
Circuits and Systems, 2000. IEEE APCCAS 2000. The 2000 IEEE Asia-Pacific Cor on , 4-6 Dec. 2000
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[Abstract] [PDF Full-Text (296 KB)] **IEEE CNF**

2 **Near fine grain parallel processing of circuit simulation using direct m**
Maekawa, Y.; Nakano, K.; Takai, M.; Kasahara, H.;
Communications, Computers, and Signal Processing, 1995. Proceedings. IEEE P Rim Conference on , 17-19 May 1995
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3 **Gate array or microcontroller? The engineers dilemma. A 4-bit microcontroller replacement case study**
Mulroy, T.J.;
Microprocessor or ASIC - Choice and Implementation, IEE Colloquium on , 21 D

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4 **Code generation for the AT&T DSP32**
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5 **HW/SW codesign for embedded telecom systems**
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Computer Design: VLSI in Computers and Processors, 1994. ICCD '94. Proceedi
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6 **A methodology for control-dominated systems codesign**
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7 **A unified scheduling model for high-level synthesis and code generati**
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8 **Constraint driven code selection for fixed-point DSPs**
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11 **Critical performance path analysis, and efficient code generation issu the Seamless architecture**
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26 **Evaluation of protocols from formal specifications: a case study with**
Sherif, M.H.; Krishnakumar, A.S.;
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